

STN

Search History

(HCAPLUS, INSPIC, JP20, USPTAII, INTPADOC)

5/8/2007

=> d 116 1-13 abs,bib

L16 ANSWER 1 OF 13 HCAPLUS COPYRIGHT 2007 ACS on STN

AB A method of producing a Si wafer having a crystal orientation <110> from a Si single-crystal ingot grown by an FZ method is described, which is characterized in that an FZ Si single-crystal ingot is grown by being made dislocation-free by a Dash necking method using a seed crystal having its crystal axis inclined a specified angle from a crystal orientation <110>, and the FZ Si single-crystal ingot thus grown is slice-cut at the just angle of a crystal orientation <110> to produce a Si wafer having a crystal orientation <110>. Accordingly, provided are a method of producing a Si wafer having a crystal orientation <110> from a Si single-crystal ingot made dislocation-free at a high success rate by using a Dash necking method by an FZ method, and a Si wafer having a crystal orientation <110>.

AN 2005:74225 HCAPLUS

DN 142:166077

TI Method of producing silicon wafer and silicon wafer

IN Yoshizawa, Ken

PA Shin-Etsu Handotai Co., Ltd. Japan

SO PCT Int. Appl., 19 pp.

CODEN: PIXXD2

DT Patent

LA Japanese

FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI WO 2005007940	A1	20050127	WO 2004-JP9921	20040712
W:				
AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NA, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RU, SC, SD, SE, SG, SK, SL, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, YU, ZA, ZM, ZW				
RW:				
BW, GH, GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW, AM, AZ, BY, KG, KZ, MD, RU, TJ, TM, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IT, LU, MC, NL, PL, PT, RO, SE, SI, SK, TR, BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG				
JP 2005041740	A	20050217	JP 2003-278483	20030723
EP 1650330	A1	20060426	EP 2004-747388	20040712
R: DE				
US 2006174820	A1	20060810	US 2006-565108	20060119
PRAI JP 2003-278483	A	20030723		
WO 2004-JP9921	W	20040712		

RE.CNT 7 THERE ARE 7 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L16 ANSWER 2 OF 13 USPTAFULL on STN

AB The present invention are a method for producing a silicon wafer having a crystal orientation <110> from a silicon single crystal ingot grown by a Floating Zone method (FZ method), wherein, at least an FZ silicon single crystal ingot is grown by being made to be dislocation-free by Dash Necking method using a seed crystal having its crystal axis inclined at a specified angle from a crystal orientation <110>, and the grown FZ silicon single crystal ingot is sliced at the just angle of a crystal orientation <110> to produce a silicon wafer having a crystal

orientation <110>, and a silicon wafer produced by the method. Thereby, there are provided a method for producing a silicon wafer having a crystal orientation <110> from a silicon single crystal ingot made to be dislocation-free at a high success rate by using Dash Necking method by FZ method, and a silicon wafer having an crystal orientation <110>.

CAS INDEXING IS AVAILABLE FOR THIS PATENT.

AN 2006:205844 USPATFULL
TI Method for producing silicon wafer and silicon wafer
IN Yoshizawa, Ken, Niigata, JAPAN
PA SHIN-ETSU HANDOTAI CO., LTD, Tokyo, JAPAN, 100-0005 (non-U.S. corporation)
PI US 2006174820 A1 20060810
AI US 2004-565108 A1 20040712 (10)
WO 2004-JP9921 20040712
20060119 PCT 371 date
PRAI JP 2003-278483 20030723
DT Utility
FS APPLICATION
LREP OLIFF & BERRIDGE, PLC, P.O. BOX 19928, ALEXANDRIA, VA, 22320, US
CLMN Number of Claims: 9
ECL Exemplary Claim: 1-4
DRWN 3 Drawing Page(s)
LN.CNT 538

CAS INDEXING IS AVAILABLE FOR THIS PATENT.

L16 ANSWER 3 OF 13 USPATFULL on STN

AB A silicon single crystal is produced by crucible-free float zone pulling, has a diameter of at least 200 mm over a length of at least 200 mm and is free of dislocations in the region of this length. A silicon wafer is separated from the silicon single crystal by a process for producing the silicon single crystal. The silicon single crystal is produced by crucible-free float zone pulling in a receptacle, in which an atmosphere of inert gas and nitrogen exerts a pressure of 1.5-2.2 bar, the atmosphere being continuously exchanged, with the volume of the receptacle being exchanged at least twice per hour. A flat coil with an external diameter of at least 220 mm is inserted in order to melt a stock ingot. The single crystal is pulled at a rate in a range from 1.4-2.2 mm/min and is periodically rotated through a sequence of rotation angles. The direction of rotation is changed, after each rotation, by a rotation angle belonging to the sequence, a change in the direction of rotating defining a turning point on the circumference of the single crystal, and at least one recurring pattern of turning points is formed, in which the turning points are distributed on straight lines which are oriented parallel to the z-axis and are uniformly spaced apart from one another.

CAS INDEXING IS AVAILABLE FOR THIS PATENT.

AN 2003:34847 USPATFULL
TI Silicon single crystal produced by crucible-free float zone pulling
IN Altmannshofer, Ludwig, Massing, GERMANY, FEDERAL REPUBLIC OF
Grundner, Manfred, Burghausen, GERMANY, FEDERAL REPUBLIC OF
Virbulis, Janis, Burghausen, GERMANY, FEDERAL REPUBLIC OF
PA Wacker Siltronic Gesellschaft Fur Halbleitermaterialien AG (non-U.S. corporation)
PI US 2003024469 A1 20030206
US 6840998 B2 20050111
AI US 2002-201431 A1 20020723 (10)
PRAI DE 2001-10137856 20010802

DT Utility
FS APPLICATION
LREP WILLIAM COLLARD, COLLARD & ROE, P.C., 1077 NORTHERN BOULEVARD, ROSLYN,
NY, 11576
CLMN Number of Claims: 18
ECL Exemplary Claim: 1
DRWN 6 Drawing Page(s)
LN.CNT 451
CAS INDEXING IS AVAILABLE FOR THIS PATENT.

L16 ANSWER 4 OF 13 USPATFULL on STN

AB An n-type wafer is provided having a <111> crystal axis in which the resistivity distribution in the surface of the wafer is uniform. The wafer is suitable for use in, e.g., a zener diode. A method is provided for growing a single crystal of n-type silicon doped with a group V element such as phosphorus using the Czochralski method or the floating zone melting (FZ) method wherein the center axis of the silicon single crystal is tilted by a tilt angle of 1-6 degrees from the <111> crystal axis. The silicon single crystal is sliced obliquely at the angle corresponding to the tilt angle to yield an n-type wafer having a <111> crystal axis.

CAS INDEXING IS AVAILABLE FOR THIS PATENT.

AN 2002:232642 USPATFULL
TI Silicon wafer and method for producing the same
IN Ito, Makoto, Saga-shi, JAPAN
PI US 2002124791 A1 20020912
AI US 2000-571890 A1 20000516 (9)
RLI Division of Ser. No. US 1998-216853, filed on 21 Dec 1998, GRANTED, Pat. No. US 6086670
PRAI JP 1997-367434 19971224
DT Utility
FS APPLICATION
LREP Oblon Spivak McClelland Maier & Neustadt P C, Fourth Floor, 1755 Jefferson Davis Highway, Arlington, VA, 22202
CLMN Number of Claims: 17
ECL Exemplary Claim: 1
DRWN 1 Drawing Page(s)
LN.CNT 475
CAS INDEXING IS AVAILABLE FOR THIS PATENT.

L16 ANSWER 5 OF 13 USPATFULL on STN

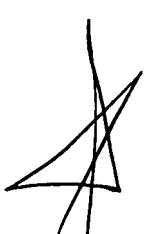
AB An n-type wafer is provided having a <111> crystal axis in which the resistivity distribution in the surface of the wafer is uniform. The wafer is suitable for use in, e.g., a zener diode. A method is provided for growing a single crystal of n-type silicon doped with a group V element such as phosphorus using the Czochralski method or the floating zone melting (FZ) method wherein the center axis of the silicon single crystal is tilted by a tilt angle of 1-6 degrees from the <111> crystal axis. The silicon single crystal is sliced obliquely at the angle corresponding to the tilt angle to yield an n-type wafer having a <111> crystal axis.

CAS INDEXING IS AVAILABLE FOR THIS PATENT.

AN 2000:87503 USPATFULL
TI Silicon wafer and method for producing the same
IN Ito, Makoto, Saga, Japan
PA Sumitomo Sitix Corporation, Amagasaki, Japan (non-U.S. corporation)
PI US 6086670 20000711
AI US 1998-216853 19981221 (9)
PRAI JP 1997-367434 19971224
DT Utility

FS Granted
EXNAM Primary Examiner: Utech, Benjamin L.; Assistant Examiner: Anderson, Matthew
LREP Oblon, Spivak, McClelland, Maier & Neustadt, P.C.
CLMN Number of Claims: 5
ECL Exemplary Claim: 1
DRWN 5 Drawing Figure(s); 1 Drawing Page(s)
LN.CNT 451
CAS INDEXING IS AVAILABLE FOR THIS PATENT.

L16 ANSWER 6 OF 13 USPATFULL on STN



AB The invention comprises a combination of a low resistivity, or electrically conducting, silicon layer that is transparent to long or short wavelength photons and is attached to the backside of a photon-sensitive layer of silicon, such as a silicon wafer or chip. The window is applied to photon sensitive silicon devices such as photodiodes, charge-coupled devices, active pixel sensors, low-energy x-ray sensors and other radiation detectors. The silicon window is applied to the back side of a photosensitive silicon wafer or chip so that photons can illuminate the device from the backside without interference from the circuit printed on the frontside. A voltage sufficient to fully deplete the high-resistivity photosensitive silicon volume of charge carriers is applied between the low-resistivity back window and the front, patterned, side of the device. This allows photon-induced charge created at the backside to reach the front side of the device and to be processed by any circuitry attached to the front side. Using the inventive combination, the photon sensitive silicon layer does not need to be thinned beyond standard fabrication methods in order to achieve full charge-depletion in the silicon volume. In one embodiment, the inventive backside window is applied to high resistivity silicon to allow backside illumination while maintaining charge isolation in CCD pixels.

CAS INDEXING IS AVAILABLE FOR THIS PATENT.

AN 2000:18670 USPATFULL
TI Low-resistivity photon-transparent window attached to photo-sensitive silicon detector
IN Holland, Stephen Edward, Hercules, CA, United States
PA The Regents of the University of California, Oakland, CA, United States (U.S. corporation)
PI US 6025585 20000215
AI US 1997-961868 19971031 (8)
DT Utility
FS Granted
EXNAM Primary Examiner: Lee, John R
LREP Martin, Paul R., Sartorio, Henry P., Aston, David J.
CLMN Number of Claims: 41
ECL Exemplary Claim: 1
DRWN 8 Drawing Figure(s); 6 Drawing Page(s)
LN.CNT 1617
CAS INDEXING IS AVAILABLE FOR THIS PATENT.

L16 ANSWER 7 OF 13 USPATFULL on STN

AB A silicon semiconductor wafer is constructed from three mutually inclined monocrystalline regions (6, 7, 8) which form three circular sectors of the wafer whose interfaces and boundary lines consequently extend radially with respect to one another and form angles (W6, W7, W8) of less than 180° with one another. In this arrangement, two of the interfaces are first-order twin grain boundaries between two <111> crystal planes in each case. The silicon semiconductor wafer is used to produce inexpensive high-performance solar cells.

AN 97:122694 USPATFULL
TI Silicon semiconductor wafer solar cell and process
for producing said wafer
IN Endros, Arthur, Munchen, Germany, Federal Republic of
Martinelli, Giuliano, Ferrara, Italy
PA Siemens Solar GmbH, Munich, Germany, Federal Republic of (non-U.S.
corporation)
PI US 5702538 19971230
WO 9517016 19950622
AI US 1996-656348 19960614 (8)
WO 1994-DE1489 19941214
19960614 PCT 371 date
19960614 PCT 102(e) date
PRAI DE 1993-4343296 19931217
DT Utility
FS Granted
EXNAM Primary Examiner: Weisstuch, Aaron
LREP Hill, Stedman & Simpson
CLMN Number of Claims: 11
ECL Exemplary Claim: 1
DRWN 10 Drawing Figure(s); 2 Drawing Page(s)
LN.CNT 600

L16 ANSWER 8 OF 13 USPATFULL on STN

AB A semiconductor substrate is formed by irradiating a semiconductor
substrate with radioactive ray so as to generate lattice defects therein
for making the entire substrate semi-insulating and then rendering only
the surface of the thus irradiated substrate semiconductive, so that a
semiconductor device is produced by using the substrate thus formed.

CAS INDEXING IS AVAILABLE FOR THIS PATENT.

AN 84:49649 USPATFULL
TI Method of making semiconductor MOSFET device by bombarding with
radiation followed by beam-annealing
IN Sugano, Takuo, Tokyo, Japan
Vu, Ho Q., Tokyo, Japan
PA Tokyo University, Tokyo, Japan (non-U.S. corporation)
PI US 4469527 19840904
AI US 1981-326253 19811201 (6)
PRAI JP 1981-93735 19810619
DT Utility
FS Granted
EXNAM Primary Examiner: Roy, Upendra
LREP Sughrue, Mion, Zinn, Macpeak and Seas
CLMN Number of Claims: 10
ECL Exemplary Claim: 1
DRWN 38 Drawing Figure(s); 9 Drawing Page(s)
LN.CNT 812

CAS INDEXING IS AVAILABLE FOR THIS PATENT.

L16 ANSWER 9 OF 13 USPATFULL on STN

AB Polycrystalline and amorphous semiconductors can be annealed using a
laser or electron beam to restore or obtain crystal order by epitaxial
regrowth on a crystal substrate. When the annealing occurs by liquid
phase epitaxy, the presence and lifetime of a molten state at the region
being annealed can be used to control the annealing process. Various
control mechanisms are described.

CAS INDEXING IS AVAILABLE FOR THIS PATENT.

AN 79:25278 USPATFULL
TI Control techniques for annealing semiconductors
IN Auston, David H., Mountainside, NJ, United States
Golovchenko, Jene A., Basking Ridge, NJ, United States
Slusher, Richard E., Lebanon, NJ, United States

Surko, Clifford M., Martinsville, NJ, United States
Venkatesan, Thirumalai N. C., Highland Park, NJ, United States
PA Bell Telephone Laboratories, Incorporated, Murray Hill, NJ, United States (U.S. corporation)
PI US 4155779 19790522
AI US 1978-935665 19780821 (5)
DT Utility
FS Granted
EXNAM Primary Examiner: Ozaki, G.
LREP Wilde, Peter V. D.
CLMN Number of Claims: 16
ECL Exemplary Claim: 1
DRWN 6 Drawing Figure(s); 2 Drawing Page(s)
LN.CNT 416
CAS INDEXING IS AVAILABLE FOR THIS PATENT.

L16 ANSWER 10 OF 13 USPATFULL on STN

AB A method of manufacturing a semiconductor device, in particular a monolithic integrated circuit, in which highly doped zones are provided according to a given pattern on one side of a monocrystalline silicon substrate body by local diffusion of at least one impurity in a substantially flat surface of the substrate body and the substrate surface on said side is given a profile in a pattern which corresponds to the pattern of the highly doped zones, after which an epitaxial silicon layer is provided on said side and one or more semiconductor circuit elements are then formed while using at least one photoresist step, characterized in that the substantially flat substrate surface is given a crystal orientation lying between a {001} face and an adjacent {111} face, which orientation deviates at least 10° from the said {001} face and at least 15° from said {111} face and is present in a strip within 10° from the crystallographic zone formed by the said two faces.

CAS INDEXING IS AVAILABLE FOR THIS PATENT.

AN 76:70430 USPATFULL
TI Method of retaining substrate profiles during epitaxial deposition
IN VAN DEN Brekel, Cornelis Hendricus Joannes, Eindhoven, Netherlands
PA U.S. Philips Corporation, New York, NY, United States (U.S. corporation)
PI US 4000019 19761228
AI US 1974-470387 19740516 (5)
PRAI NL 1973-6948 19730518
DT Utility
FS Granted
EXNAM Primary Examiner: Rutledge, L. Dewayne; Assistant Examiner: Saba, W. G.
LREP Trifari, Frank R., Nigohosian, Leon
CLMN Number of Claims: 3
ECL Exemplary Claim: 1
DRWN 9 Drawing Figure(s); 4 Drawing Page(s)
LN.CNT 1068
CAS INDEXING IS AVAILABLE FOR THIS PATENT.

L16 ANSWER 11 OF 13 USPAT2 on STN

AB A silicon single crystal is produced by crucible-free float zone pulling, has a diameter of at least 200 mm over a length of at least 200 mm and is free of dislocations in the region of this length. A silicon wafer is separated from the silicon single crystal by a process for producing the silicon single crystal. The silicon single crystal is produced by crucible-free float zone pulling in a receptacle, in which an atmosphere of inert gas and nitrogen exerts a pressure of 1.5-2.2 bar, the atmosphere being continuously exchanged, with the volume of the receptacle being exchanged at least twice per hour. A flat coil with an external diameter of at least 220 mm is inserted in order to melt a stock ingot. The single crystal is pulled at a rate in a range from

1.4-2.2 mm/min and is periodically rotated through a sequence of rotation angles. The direction of rotation is changed, after each rotation, by a rotation angle belonging to the sequence, a change in the direction of rotating defining a turning point on the circumference of the single crystal, and at least one recurring pattern of turning points is formed, in which the turning points are distributed on straight lines which are oriented parallel to the z-axis and are uniformly spaced apart from one another.

CAS INDEXING IS AVAILABLE FOR THIS PATENT.

AN 2003:34847 USPAT2
TI Silicon single crystal produced by crucible-free float zone pulling
IN Altmannshofer, Ludwig, Massing, GERMANY, FEDERAL REPUBLIC OF
Grundner, Manfred, Burghausen, GERMANY, FEDERAL REPUBLIC OF
Virbulis, Janis, Burghausen, GERMANY, FEDERAL REPUBLIC OF
PA Siltronic AG, Munich, GERMANY, FEDERAL REPUBLIC OF (non-U.S. corporation)
PI US 6840998 B2 20050111
AI US 2002-201431 20020723 (10)
PRAI DE 2001-10137856 20010802
DT Utility
FS GRANTED
EXNAM Primary Examiner: Norton, Nadine G.; Assistant Examiner: Anderson, Matthew
LREP Collard & Roe, P.C.
CLMN Number of Claims: 18
ECL Exemplary Claim: 1
DRWN 7 Drawing Figure(s); 6 Drawing Page(s)
LN.CNT 463

CAS INDEXING IS AVAILABLE FOR THIS PATENT.

L16 ANSWER 12 OF 13 INPADOC COPYRIGHT 2007 EPO on STN

LEVEL 1

AN 308476951 INPADOC ED 20060824 EW 200634 UP 20060824 UW 200634
TI Method for producing silicon wafer and silicon wafer.
IN YOSHIZAWA KEN
INS YOSHIZAWA KEN
INA JP
PA SHIN-ETSU HANDOTAI CO., LTD
PAS SHINETSU HANDOTAI KK
PAA JP
TL English
LA English
DT Patent
PIT USAA PATENT APPLICATION PUBLICATION (PRE-GRANT)
PI US 2006174820 AA 20060810
AI US 2006-565108 A 20060119
PRAI JP 2003-278483 A 20030723 (EDPR 20050211)
WO 2004-JP9921 W 20040712 (EDPR 20060427)

L16 ANSWER 13 OF 13 INPADOC COPYRIGHT 2007 EPO on STN

LEVEL 1

AN 261373847 INPADOC ED 20050211 EW 200506 UP 20060420 UW 200616
TI METHOD OF PRODUCING SILICON WAFER AND SILICON WAFER.
PROCEDE DE PRODUCTION DE PLAQUETTE DE SILICIUM ET PLAQUETTE DE SILICIUM.
IN YOSHIZAWA, KEN
INS YOSHIZAWA KEN
INA JP
PA SHIN-ETSU HANDOTAI CO., LTD.; YOSHIZAWA, KEN

PAS SHINETSU HANDOTAI KK; YOSHIKAWA KEN
PAA JP; JP
TL English; French
LA Japanese
DT Patent
PIT WOA1 PUBL.OF THE INT.APPL. WITH INT.SEARCH REPORT
PI WO 2005007940 A1 20050127
DS RW: BW GH GM KE LS MW MZ NA SD SL SZ TZ UG ZM ZW AM AZ BY KG KZ MD RU TJ
TM AT BE BG CH CY CZ DE DK EE ES FI FR GB GR HU IE IT LU MC NL PL PT
RO SE SI SK TR BF BJ CF CG CI CM GA GN GQ GW ML MR NE SN TD TG BF BJ
CF CG CI CM GA GN GQ GW ML MR NE SN TD TG
W: AE AE AG AL AL AM AM AM AT AT AU AZ AZ BA BB BG BG BR BR BW BY BY BZ
BZ CA CH CN CN CO CO CR CR CU CU CZ CZ DE DE DK DK DM DZ EC EC EE EE
EG EG ES ES FI FI GB GD GE GE GH GM HR HR HU HU ID IL IN IS KE KE KG
KG KP KP KP KR KR KZ KZ KZ LC LK LR LS LS LT LU LV MA MD MD MG MK MN
MW MX MX MZ MZ NA NI NI NO NZ OM PG PH PH PL PL PT PT RO RU RU SC SD
SE SG SK SK SL SL SY TJ TJ TM TM TN TR TR TT TT TZ UA UA UG UG US UZ
UZ VC VN YU YU ZA ZM ZW
AI WO 2004-JP9921 A 20040712
PRAI JP 2003-278483 A 20030723 (EDPR 20050211)
OSCA 142:166077

=> d his

(FILE 'HOME' ENTERED AT 14:04:40 ON 08 MAY 2007)

FILE 'HCAPLUS, INSPEC, JAPIO, USPATFULL, USPAT2, INPADOC' ENTERED AT
14:22:57 ON 08 MAY 2007

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L3 3103 S (110(W) ORIENTAT?)
L4 17718 S (FZ OR FLOAT? (W) ZONE#)
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L12 1 S L1 AND L2 AND L3 AND L4 AND L5 AND L7
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L14 0 S L1 AND L3 AND L4 AND L5 AND L6 AND L8
L15 0 S L1 AND L3 AND L4 AND L5 AND L6 AND L8
L16 13 S L1 AND L4 AND L5 AND L9

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=> d 112 abs,bib

L12 ANSWER 1 OF 1 USPATFULL on STN

AB A method of manufacturing a semiconductor device, in particular a monolithic integrated circuit, in which highly doped zones are provided according to a given pattern on one side of a monocrystalline silicon substrate body by local diffusion of at least one impurity in a substantially flat surface of the substrate body and the substrate surface on said side is given a profile in a pattern which corresponds to the pattern of the highly doped zones, after which an epitaxial silicon layer is provided on said side and one or more semiconductor circuit elements are then formed while using at least one photoresist step, characterized in that the substantially flat substrate surface is given a crystal orientation lying between a {001} face and an adjacent {111} face, which orientation deviates at least 10° from the said {001} face and at least 15° from said {111} face and is present in a strip within 10° from the crystallographic zone formed by the said two faces.

CAS INDEXING IS AVAILABLE FOR THIS PATENT.

AN 76:70430 USPATFULL
TI Method of retaining substrate profiles during epitaxial deposition
IN VAN DEN Brekel, Cornelis Hendricus Joannes, Eindhoven, Netherlands
PA U.S. Philips Corporation, New York, NY, United States (U.S. corporation)
PI US 4000019 19761228
AI US 1974-470387 19740516 (5)
PRAI NL 1973-6948 19730518
DT Utility
FS Granted
EXNAM Primary Examiner: Rutledge, L. Dewayne; Assistant Examiner: Saba, W. G.
LREP Trifari, Frank R., Nigohosian, Leon
CLMN Number of Claims: 3
ECL Exemplary Claim: 1
DRWN 9 Drawing Figure(s); 4 Drawing Page(s)
LN.CNT 1068
CAS INDEXING IS AVAILABLE FOR THIS PATENT.

=> d his

(FILE 'HOME' ENTERED AT 14:04:40 ON 08 MAY 2007)

FILE 'HCAPLUS, INSPEC, JAPIO, USPATFULL, USPAT2, INPADOC' ENTERED AT 14:22:57 ON 08 MAY 2007

L1 196114 S (SI OR SILICON) (8A) (WAFER#)
L2 155712 S (CRYSTAL? (6A) ORIENTAT?)
L3 3103 S (110 (W) ORIENTAT?)
L4 17718 S (FZ OR FLOAT? (W) ZONE#)
L5 5864 S (DISLOCAT? (2W) FREE OR DISLOCAT (W) FREE)
L6 124 S (DASH (2W) NECKING OR DASH (W) NECK?)
L7 29833 S (SEED (4A) CRYSTAL#)
L8 2880874 S (SLIC? OR CUT? OR DISECT? OR SAW? OR CHAMFER?)
L9 2629700 S (ANGLE#)
L10 0 S L1 AND L2 AND L3 AND L4 AND L5 AND L6 AND L7
L11 425 S L1 AND L2 AND L3
L12 1 S L1 AND L2 AND L3 AND L4 AND L5 AND L7

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